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10/508,776	09/23/2004	Yoshimasa Okabe	2004_1456A	7891

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EXAMINER
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ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _23 September 2004_.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-7_ is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) _1-7_ is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on _23 September 2004_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☒ All   b) ☐ Some * c) ☐ None of:
        1. ☒ Certified copies of the priority documents have been received.
        2. ☐ Certified copies of the priority documents have been received in Application No. _____.
        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _23 Setember 2004_.
4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1.   Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2.   The information disclosure statement (IDS) submitted on 23 September 2004 was filed after the mailing date of the same day on 23 September 2004.

The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

Claim Objections

3.   Claim 5 is objected to because of the following informalities: On line 2, "sifting" should be replaced by "shifting". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   **Claims 1-7** are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (U.S. Patent Publication number 20002/0113885A1).

6.   **Regarding claim 1,** Inoue discloses an image processing apparatus comprising an image storage section adapted to store an image, an arithmetic section adapted to generate output pixels (see abstract) by arithmetically

processing adjacent pixels consisting of M pixels adjoining in the horizontal

direction (see column 5, lines 41-44 and column 6, lines 15-16) and N pixels

adjoining in the vertical direction of the image (see column 5, lines 44 and

column 6, lines 16), the M being an integer of two or more, and the N being an

integer of one or more a first temporary storage section (column 9, line 55)

adapted to readably store the pixels ranging from a Mth pixel to a last pixel in

each of horizontal pixel lines of the image (see column 7, lines 4 and Fig.4), a

second temporary storage section (column 9, line 55) adapted to readably store

the pixels ranging from a head pixel to a (M- 1)th pixel in each of the horizontal

pixel lines of the image (see column 7, line 4 and Fig.4), and a third temporary

storage section (see column 9, lines 55) adapted to delay outputs of the pixels

stored in the first temporary storage section (see claim 8 and column 22, lines

27-35), to receive the pixels from the second temporary storage section, and to

simultaneously output the adjacent pixels consisting of the M pixels adjoining in

the horizontal direction and the N pixels adjoining in the vertical direction to the

arithmetic section (see column 6, lines 49-54 and Fig.4).

7.   **Regarding claim 2,** Inoue discloses an image processing apparatus of

claim 1, further comprising a control section wherein before the pixels for

generating a last output pixel of one of the horizontal pixel lines are stored in the

third temporary storage section, the control section reads the pixels ranging from

the head pixel to the (M-1)th pixel of the next horizontal pixel from the image

storage section to write them to the second temporary storage section (see

column 6, lines 64-67 and column 7, lines 55-60), and wherein after the pixels

for generating the last output pixel of the one of the horizontal pixel lines is

outputted from the third temporary storage section to the arithmetic section, the

control section reads the pixels ranging from the head pixel to the (M- 1)th pixel

of the next horizontal pixel line from the second temporary storage section to

write them to the third temporary storage section (column 6, lines 64-67 and

column 7, lines 55-60).

8.   **Regarding claim 3**, Inoue discloses an image processing apparatus of

claim 2, wherein the N is an integer of two or more, and wherein with respect to

the pixels belonging to the first to the Nth horizontal pixel lines of the image, the

control section repeats an operation of sequentially reading the N pixels arranged

in the vertical direction from the image storage section (see column 7,lines 64-

67) and writing the pixels in the first temporary storage section or the second

temporary storage section with shifting a reading position in the horizontal

direction (see column 7, lines 28-31 and column 8,lines 54-55).

9.   **Regarding claim 4**, Inoue discloses an image processing apparatus of

claim 3, wherein the arithmetic section generates the output pixel in every unit

time (see column 8, lines 59-61), wherein the first temporary storage section has

N RAMs (see column 9, lines 55-57 and column 22, claim 7 and line 18), and

wherein the control section reads one pixel from the image storage section and

writes the pixel to the RAM or the second temporary storage section (see column

9,lines 55-57 and column 22, claim 7 and lines 19)within the unit time when a

previous writing address of the RAM under writing is immediately before a

previous reading address, and reads plural pixels from the image storage section

and writes the pixels to the RAM and/or the second temporary storage section

within the unit when the previous writing address of the RAM under writing is an

address two or more immediately before the previous reading address (see

column 9, lines 48-55 and column 22, claim 8 and lines 27-35).

10.   **Regarding claim 5,** Inoue discloses an image processing method of

generating output pixels by arithmetically processing adjacent pixels consisting of

M pixels adjoining in a horizontal direction (see column 6, lines 15-16) and N

pixels adjoining in a vertical direction (column 6, lines 16) in an image stored in

an image storage section, M being an integer of two or more, and N being an

integer of one or more (see column 5, lines 41-44), comprising reading the pixels

from the image storage section with shifting a reading position in the horizontal

direction (column 11, lines 6-7 and column 12, lines 11) and writing the pixels in

a first temporary storage section; reading the pixel from the first temporary

storage section and writing the pixel in a third temporary storage section (see

column 11, lines 15-18); delaying output of the pixels by the third temporary

storage section so as to output the pixels consisting of the M adjacent pixels in

the horizontal direction and the N adjacent pixels in the vertical direction to an

arithmetic section (see column 22, claim 8 and lines 27-35); generating the

output pixel from the M x N pixels by the arithmetic section ; before the pixels for

generating a last output pixel in one horizontal pixel line is stored in the third

temporary storage section (see column 9, lines 55) , reading pixels ranging from

a head pixel to a (M-1)th pixel in the next horizontal pixel line from the image

storage section and writing the pixels in a second temporary storage section

(See column 7, lines 55-61); and after the pixels for generating the last output

pixel in the one horizontal pixel line are outputted from the third temporary

storage section to the arithmetic section, reading the pixels ranging from the

head pixel to the (M-1)th pixel in the next line from the second temporary storage

section and writing the pixels in the third temporary storage section (see column

6, lines 49-54 and Fig.4).

11.   **Regarding claim 6**, Inoue discloses an image processing method of

claim 5, wherein the N is an integer of two or more, and wherein the image

processing method further comprising, with respect to the plural pixels belonging

to the first to the Nth horizontal pixel lines of the image, repeating an operation of

sequentially reading the N pixels arranged in the vertical direction from the image

storage section (see column 7,lines 64-67) and writing the pixels in the first

temporary storage section or the second temporary storage section with shifting

(see column 12, lines 11) a reading position in the horizontal direction (see

column 7, lines 28-31 and column 8,lines 54-55).

12.   **Regarding claim 7**, Inoue discloses an image processing method of claim

5, wherein the arithmetic section generates one output pixel in every unit time

(see column 8,lines 58-61), wherein the first temporary storage section has N

RAMs (see column 9, lines 55-57 and column 22, claim 7 and line 18), wherein

one pixel is read from the image storage section and written to the RAM (see

column 9,lines 55-57) or the second temporary storage section in the unit time

when the previous writing address of the RAMs under writing is immediately

before the previous reading address (see column 22, claim 8 and lines 27-35),

and wherein the plural pixels are read from the image storage section and written

to the RAMs or the second temporary storage section in the unit time when the

previous writing address of said RAMs under writing is an address two or more

before the previous reading address (see column 9, lines 48-55).

Conclusion

13.   The prior art made of record and not relied upon is considered pertinent

to applicant's disclosure. Egawa (U.S.Patent number 5,138,460) discloses

display device for displaying an image to photograph such as a portion of an

object.

Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Aklilu k. Woldemariam whose telephone

number is 571-270-3247. The examiner can normally be reached on Monday-

Thursday 6:30 a.m-5:00 p.m EST.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Alexander Eisen can be reached on 571-272-7687. The

fax phone number for the organization where this application or proceeding is

assigned is 571-273-8300.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

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free). If you would like assistance from a USPTO Customer Service

Representative or access to the automated information system, call 800-786-

9199 (IN USA OR CANADA) or 571-272-1000.

Alexander Eisen
SPE
Art Unit 2609

A.W.

5/8/2007